Preliminary Specifications Ver1.3

Product Name THB7128-E

1．Case Outline：19 pins (See attached case outline dimensions.)
2．Function ： PWM current control stepping motor driver

3．Application ： Industrial equipment etc.

4．Features：

- Output on-resistance (High side 0.3 Ω, Low side 0.25 Ω, Total 0.55 Ω; Ta = 25℃, I_O = 2.5A)
- VMmax=40V(DC)，Iopmax=3.3A
- 2, 1-2, W1-2, 2W1-2, 4W1-2, 8W1-2, 16W1-2, 32W1-2 phase excitation are selectable
- With built-in automatic half current maintenance energizing function
- Over current protection circuit
- Thermal shutdown circuit
- Input pull down resistance
- With reset pin and enable pin

5．Absolute Maximum Ratings／Tc=25℃

Parameter	Symbol	Conditions	Ratings	Unit
supply voltage	VMmax		40	V
Peak output current	Iopmax		3.3	A
Logic input voltage	VINmax		6	V
VREF input voltage	VREFmax		3	V
Operating substrate temperature	Tc		-30 to +105	℃
Storage temperature	Tstg		-40 to +125	℃

6．Allowable Operating Ranges／Ta=25℃

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage range	VM		9 to 32	V
Logic input voltage range	VIN		0 to 5	V
VCC input voltage range	VCC		0 to 5	V
VREF input voltage range	VREF		0 to 3	V
Output current1	Io1	1-2Phase-ex，Tc≦90℃	3.0	A
Output current2	Io2	1-2Phase-ex，Tc=105℃	2.5	A
Output current3	Io3	2Phase-ex，Tc=105℃	1.8	A

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7．Electrical Characteristics／Tc=25℃, VM=24V, VREF=1.5V

Parameter	Symbol	Conditions	Ratings			Unit
			min.	typ.	max.	
Standby mode current drain	IMstn	VCC="L"		100		μA
Current drain	IM	VCC＝"H"， ENABLE="H" No Load		3.3	4.6	mA
Thermal shutdown temperature	TSD	Design guarantee	150	180	210	℃
Thermal hysteresis width	ΔTSD	Design guarantee		40		℃

8. Block diagram
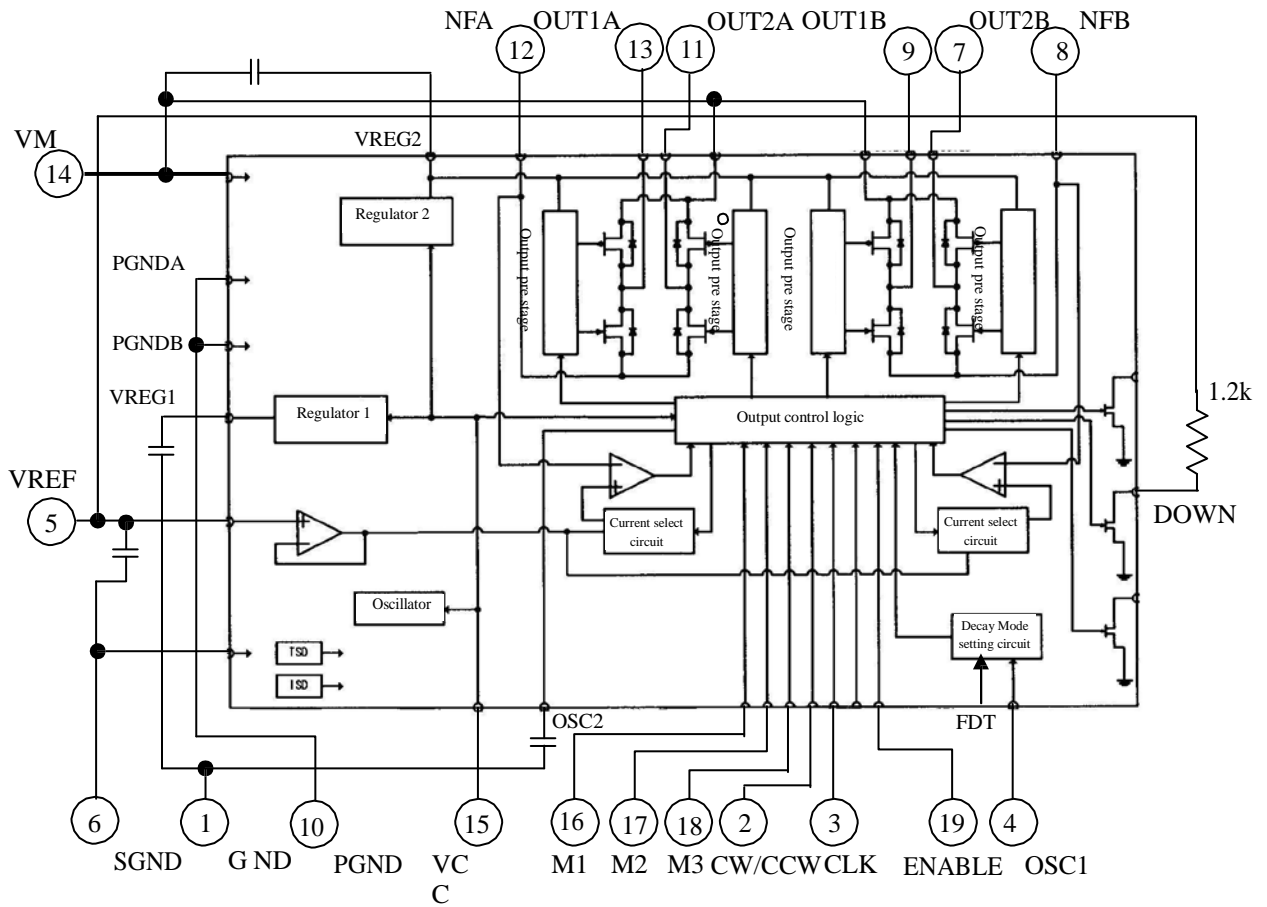
9. Application Circuit Example

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No.3
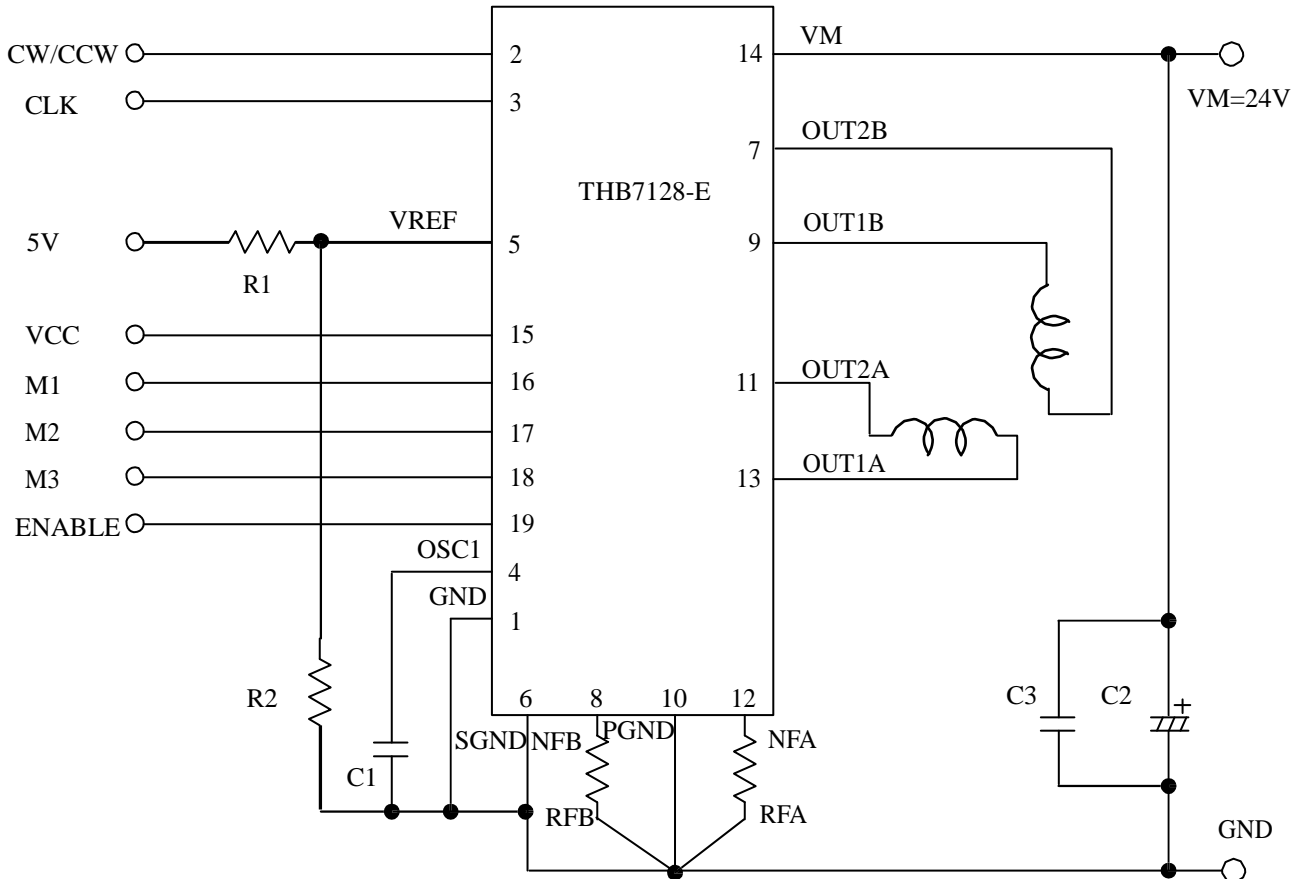
10．Pin Functions

Pin No.	Pin symbol	Pin Functions
1	GND	Circuit GND
2	CW/CCW	Forward / Reverse signal input
3	CLK	Clock pulse signal input
4	OSC1	Chopping frequency setting capacitor connection
5	VREF	Constant-current control reference voltage input
6	SGND	Signal GND
7	OUT2B	B phase OUTB output
8	NFB	B phase current sense resistance connection
9	OUT1B	B phase OUTA output
10	PGND	Power GND
11	OUT2A	A phase OUTB output
12	NFA	A phase current sense resistance connection
13	OUT1A	A phase OUTA output
14	VM	Motor supply connection
15	VCC	Chip enable input
16	M1	Excitation-mode switching pin
17	M2	
18	M3	
19	ENABLE	Output enable signal input

11. Description of functions

(1) Excitation setting method

Set the excitation setting as shown in the following table by setting M1 pin, M2 pin and M3 pin

Input signal			MODE（Excitation）	Initial position	
M3	M2	M1		A phase current	B phase current
L	L	L	2 Phase	100%	-100%
L	L	H	1-2 Phase	100%	0%
L	H	L	W1-2 Phase	100%	0%
L	H	H	2W1-2 Phase	100%	0%
H	L	L	4W1-2 Phase	100%	0%
H	L	H	8W1-2 Phase	100%	0%
H	H	L	16W1-2 Phase	100%	0%
H	H	H	32W1-2 Phase	100%	0%

The initial position is also the default state at start-up and excitation position at counter-reset in each excitation mode

(2) Output current setting

Output current is set as shown below by the VREF pin (applied voltage) and a resistance value between NFA (B) pin and GND.

I_{OUT} = (VREF / 5) / NFA (B) resistance
* The setting value above is a 100% output current in each excitation mode.

(Example) When VREF=1.5V and NFA (B) resistance is 0.3 Ω, the setting current is shown below.
I_{OUT} = (1.5 V / 5) / 0.3 Ω = 1.0 A

(3) Chip enable terminal/ VCC function

When Chip enable terminal/ V_{CC} pin is at low levels, the IC enters stand-by mode, all logic is reset and output is turned OFF.
When Chip enable terminal/ V_{CC} pin is at high levels, the stand-by mode is released

(4) Step pin function

CLK pin step signal input allows advancing excitation step

Input		Operation
V_{CC}	CLK	
L	*	Stand-by mode
H	⌐⌐↑	Excitation step feed
H	⌐⌐↓	Excitation step hold

(5) Forward / reverse switching function

CW/CCW	Operation
L	CW
H	CCW

(6) Output enable function

When the ENABLE pin is set Low, the output is forced OFF and goes to high impedance. However, the internal logic circuits are operating, so the excitation position proceeds when the CLK is input. Therefore, when ENABLE pin is returned to High, the output level conforms to the excitation position proceeded by the CLK input.

(7) DECAY mode

The DECAY mode of the output current becomes only MIXED DECAY.

(8) Chopping frequency setting function

Chopping frequency is set as shown below by a capacitor between OSC1 pin and GND.

$Fch = 1 \diagup (C1+20pF \diagup 10 \times 10^{-6})$ (Hz)

(Example) When Cosc1=100pF, the chopping frequency is shown below.

$Fch = 1 \diagup ((20+100) \times 10^{-12} \diagup 10 \times 10^{-6})$ (Hz) = 83.3 (kHz)

Note

・The 20pF is a stray capacitance which is involved by the package of THB7128-E.

(9) Output short-circuit protection circuit

Build-in output short-circuit protection circuit makes output to enter in stand-by mode. This function prevents the IC from damaging when the output shorts circuit by a voltage short or a ground short, etc. When output short state is detected, short-circuit detection circuit starts the operating and output is once turned OFF. After the timer latch time (typ: 256μs), output is turned ON again. Still the output is at short state, the output is turned OFF and fixed in stand-by mode.

When output is fixed in stand-by mode by output short protection circuit, output is released the latch by setting Chip enable terminal/ V_{CC}="L"
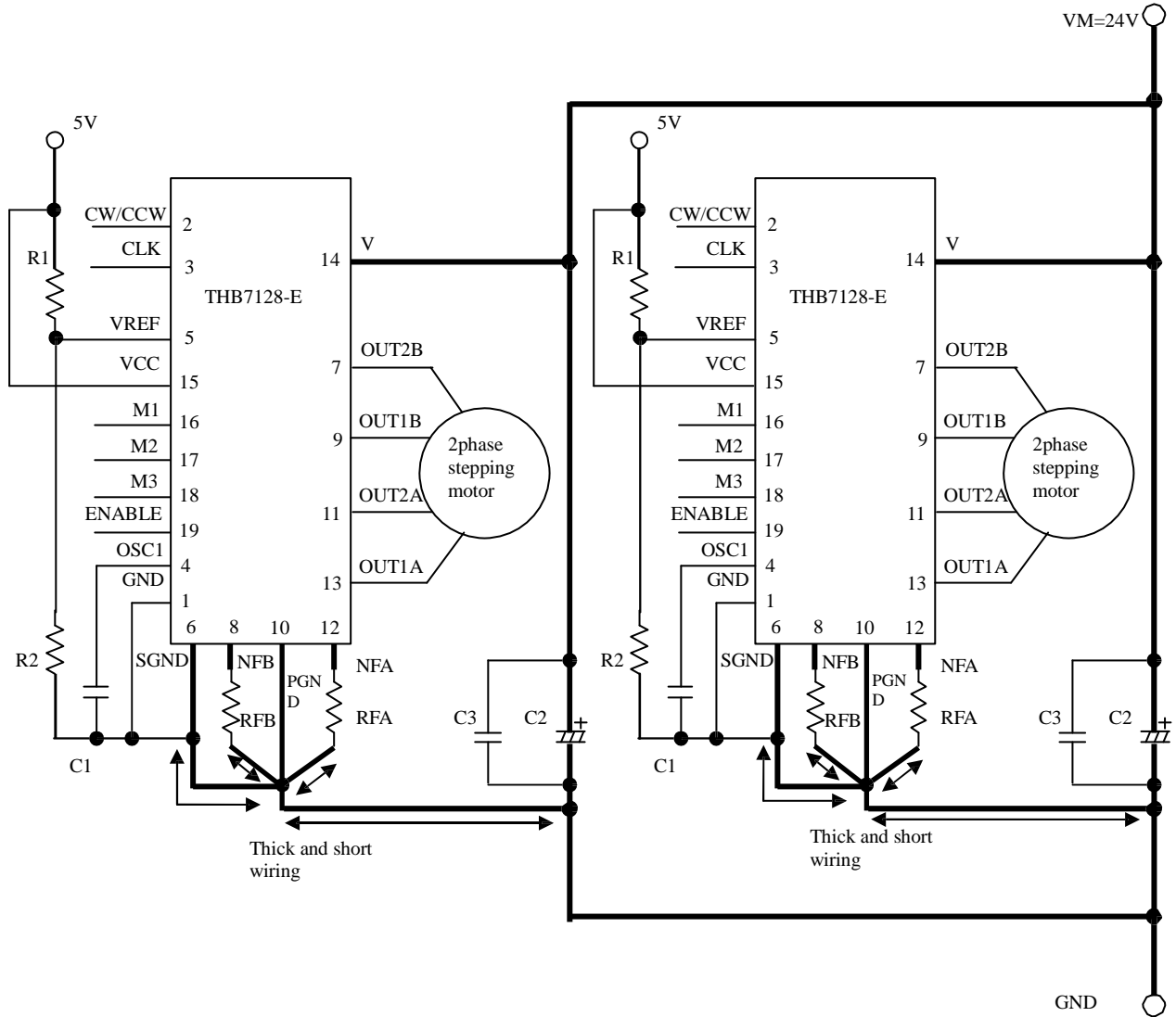
(10) Output current tolerance

THB7128-E   Output current tolerance   Io－Tc
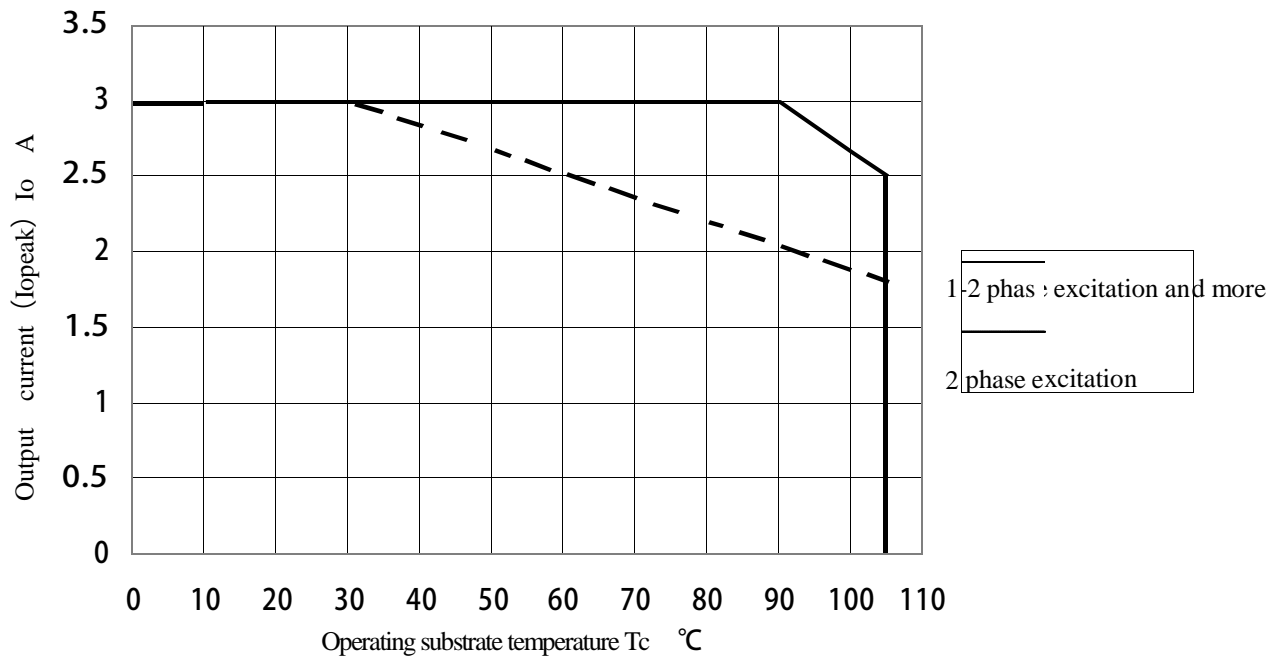
(11) When mounting multiple drivers on a single PC board

When mounting multiple drivers on a single PC board, the GND design should mount a VCC decoupling capacitor, C2 and C3, for each driver to stabilize the GND potential of the other drivers. The key wiring points are as follows.

Package Outline Diagram

Product Name   THB7128-E

$4.5^{+0.15}_{-0.05}$

⟨5.0⟩

⟨5.0⟩

11.0

⟨3.5⟩

1.0

0.5±0.05

18×1.0⁻

4.2

8.2
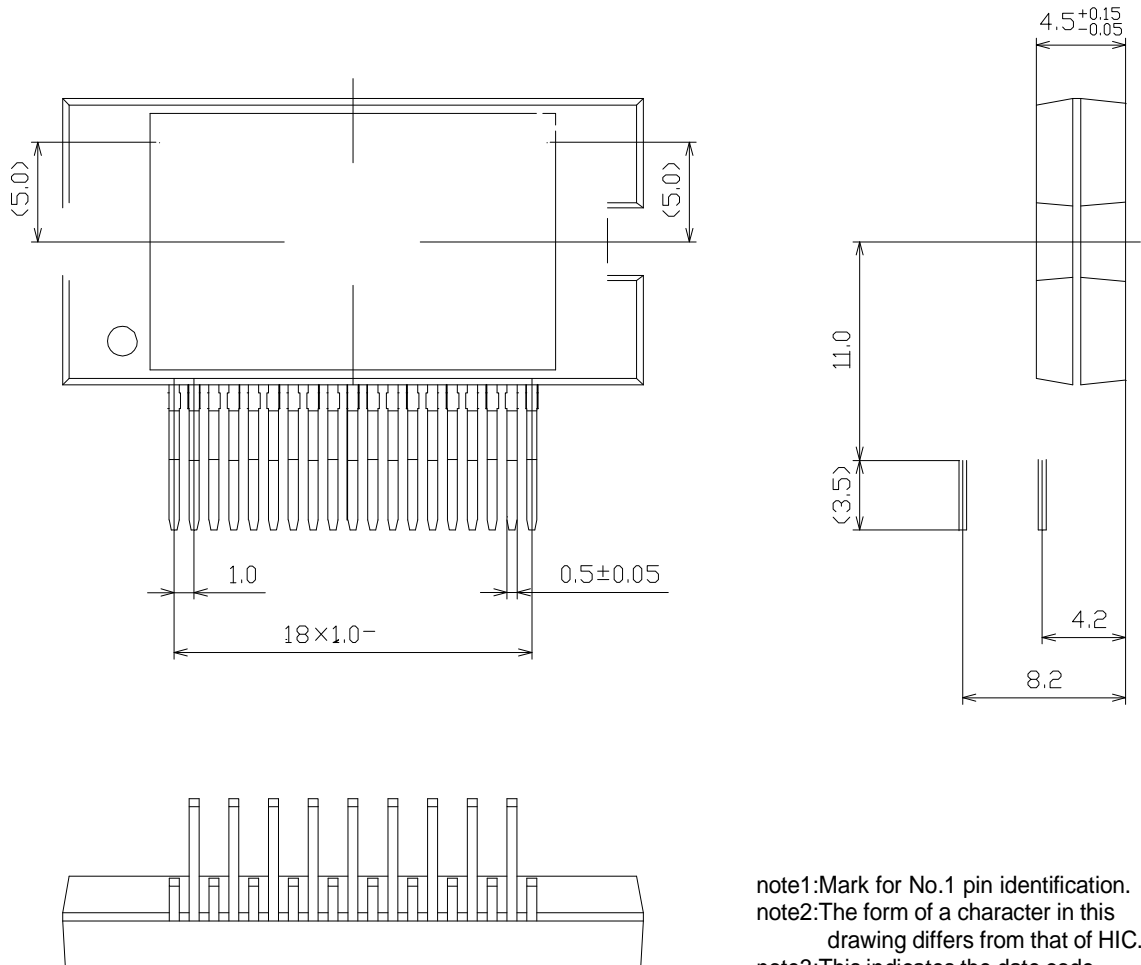
note1: Mark for No.1 pin identification.
note2: The form of a character in this
        drawing differs from that of HIC.
note3: This indicates the date code.
        The form of a character in this
        drawing differs from that of HIC.

No.	Part Name	Material	Treatment
①	Case	EPOXY	
②	Substrate	IMST Substrate	
③	Lead Frame	Cu	Sn

Unit	mm	
Tolerance	±0.4	
Don't scale this drawing.		
Control No.	016−09−0083	

Oct.21.2009	Newly prepared	Machida	Sakai
Date	Revision	In charge	Approval

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No.8